Ahmad Khan

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Education

University of British Columbia Expected May 2027
Bachelor of Applied Science – Computer Engineering (4th Year) *Vancouver, BC*

Technical Skills

Languages: SystemVerilog, Verilog, C/C++, Python, MIPS assembly, Bash
Design: RTL design, microarchitecture, datapath and control, FSM design, clock-domain crossing, fixed-point (Q-format) arithmetic, synthesis, static timing analysis, timing closure
Verification: UVM 1.2 (driver, monitor, sequencer, reactive responder, scoreboard), golden-model checking, randomized stimulus with back-pressure and latency injection, FSM state/transition coverage, SignalTap
Tools & Interfaces: Quartus Prime, Questa, ModelSim, Platform Designer, Nios II SBT, Git, Linux, GDB; Avalon-MM slave and master (waitrequest/readdatavalid), memory-mapped I/O, on-chip M10K RAM, EPCQ serial flash, JTAG UART, PS/2, I^2C
Coursework: CPEN 411 (Computer Architecture), ELEC 402 (VLSI Design), CPEN 311 (Digital Systems Design), CPEN 331 (Operating Systems), CPEN 491 (Capstone)

Projects

Fixed-Point Neural Network Accelerator ***(GitHub)*** | *SystemVerilog, UVM, Questa* Dec 2025 – Jul 2026

- Designed a Q8.8 dense-layer MAC accelerator in SystemVerilog on a Cyclone V DE1-SoC with Avalon-MM slave (7 CSRs) and master interfaces, driven by a Nios II/e at 50 MHz: **473 ALMs**, 495 FFs, 4 DSP blocks, **Fmax 73 MHz** with +6.3 ns setup slack at 50 MHz.
- Ran a 784-16-16-10 MNIST inference in **78k cycles (1.56 ms)** in simulation; trained the MLP in Python and exported Q8.8 weights and biases as .mif, with the bit-accurate fixed-point model scoring **95.27%** on the 10,000-image test set, **0.04** points below float32.
- Built a UVM 1.2 testbench (CSR agent, reactive Avalon-MM memory responder with programmable latency and back-pressure, golden-model scoreboard, FSM transition checker): 7 tests, 141 outputs checked, **13/13 states and 20/21 transitions** covered.
- Found a duplicate-read bug under 30% random waitrequest back-pressure that every directed test had missed, and root-caused it to read re-assertion during the readdatavalid wait.

Dual-Core RC4 Key-Search Engine ***(GitHub)*** | *SystemVerilog, Questa, SignalTap* Jun 2025 / Sep 2026

- Implemented RC4 key scheduling, PRGA, and decrypt as three cooperating FSMs (11/17/9 states) with explicit handshaking over single-port synchronous M10K RAM, at **4,299 cycles per candidate key** (11.6k keys/s at 50 MHz).
- Partitioned the 2^{22} key space across two cores searching from opposite ends with early exit on the first plausible-ASCII plaintext, halving worst-case search from **6.0 to 3.0 minutes**: 1,162 ALMs, Fmax 79 MHz; verified in Questa against known-key ciphertexts from both halves and on DE1-SoC hardware with SignalTap.

Real-Time FPGA Audio Player ***(GitHub)*** | *Verilog, CDC, Avalon-MM* Jun 2025

- Streamed 2 MiB of 8-bit samples from EPCQ serial flash over Avalon-MM with waitrequest/readdatavalid handshaking to a WM8731 codec, under PS/2 play, stop, forward, backward, and restart control.
- Closed a **27 MHz to 50 MHz clock-domain crossing** with an async-trap and two-flop synchronizer that converts the divided sample clock into a single-cycle tick, eliminating dropped and doubled samples.

OS/161 Kernel | *C, MIPS, sys161, GDB* Sep – Dec 2025

- Implemented fork, execv, waitpid, _exit, getpid, and sbrk in C with a global PID table, per-process wait condition variables, and argv marshalling through copyin/copyout onto the user stack (solo).
- Replaced DUMBVM with a two-level page table and physical-frame tracker: lazy page allocation on first fault, R/W/X permission enforcement, TLB refill with random eviction, and heap growth via sbrk (solo).
- Built locks and condition variables on wait channels, and the open/read/write/lseek/close/dup2 layer over a per-process descriptor table with reference-counted shared open-file objects.